UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,354	07/14/2003	Tao Cheng,	MTKP0024USA	1353

27765 7590 05/19/2006

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
ROMAN, LUIS ENRIQUE	
ART UNIT	**PAPER NUMBER**
2836	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,354	CHENG, ET AL.	
	Examiner	Art Unit	
	Luis Roman	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 6-13* is/are rejected.

7)☒ Claim(s) *4 and 5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant amendment filed on 03/16/06 has been entered. Accordingly claims 2-12 have been kept original, claim 1 has been amended and no claims have been cancelled. New claim 13 was added. It also included remarks/arguments.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Diaz et al. (US 5450267).

Regarding claim 1 Diaz et al. discloses an electrostatic discharge protection circuit (Abstract) comprising: a Darlington circuit comprising a input end and an output end (Fig. 2 elements Qd, Q1); and an N-type channel metal-oxide semiconductor (NMOS) transistor (Fig. 2 element M1), a drain of the NMOS transistor connected to the input end of the Darlington circuit (Fig. 2 connected both to element 22) a source of the NMOS transistor connected to a control end of the Darlington circuit (Fig. 2 node v2), a gate of the NMOS transistor connected to the output end of the Darlington circuit. (Fig. 2 connected both to element 26).

Diaz et al. does not disclose the Darlington being a npn one.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Diaz et al. pnp Darlington with a npn Darlington, because this

requires only routine skill in the art depending on the characteristics required for the apparatus and the specific overvoltages present in the circuit.

Claims 1, 10, 11 & 12 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ker et al. (US 6072219) in view of Voldman et al. (US 6549061).

Regarding claim 1 Ker et al. discloses an electrostatic discharge protection circuit (Abstract) comprising an N-type channel metal-oxide semiconductor (NMOS) transistor (Col. 5 lines 37-53 & Fig. 4 element N1), a drain of the NMOS transistor connected to a clamp circuit (Fig. 4 elements B1, F1), a source of the NMOS transistor connected to a control end of the transistor circuit (Fig. 4 elements B1, F1), a gate of the NMOS transistor connected to the output end of the transistor circuit (Fig. 4 element Vss).
Ker et al. does not disclose wherein the clamp circuit is an npn Darlington circuit comprising a input end and an output end.
Voldman et al. teaches wherein a clam circuit is an npn Darlington circuit (Fig. 6 element 604) comprising a input end (Fig. 6 element 210) and an output end (Fig. 6 element 212), the output end of the npn Darlington circuit being grounded (Fig. 6 element 212).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Ker et al. device with the Voldman et al. Darlington features. Both teachings are in the ESD area, which have a main purpose to reduce the impedance between the input pad and the power source (i.e. discharge of current between the input to the power source). Furthermore, a Darlington offers the advantage of driving/supporting higher magnitudes of current than a single transistor, because it has a gain equals to $\beta^2 = \beta_1 . \beta_2$ (where $\beta 1$ and $\beta 2$ correspond to the gains of each transistor).

Regarding claim 10 Ker et al. in view of Voldman et al. discloses the electrostatic discharge protection circuit of claim 1.
Ker et al. further discloses wherein the input end of the npn Darlington circuit is connected to an input end of another circuit (Fig. 4 element IP).

Regarding claim 11 Ker et al. in view of Voldman et al. discloses the electrostatic discharge protection circuit of claim 1.
Voldman et al. further discloses wherein the input end of the npn Darlington circuit is connected to a voltage source (Fig. 6<604> element V1 Rail <210>).

Regarding claim 12 Ker et al. in view of Voldman et al. discloses the electrostatic discharge protection circuit of claim 1.

Ker et al. in view of Voldman et al. further discloses comprising a pnp Darlington circuit, an input end of the pnp Darlington circuit connected to the input end of the npn Darlington circuit, an output end of the pnp Darlington circuit connected to a voltage source, and a P-type channel metal-oxide semiconductor (PMOS) transistor, a drain of the PMOS transistor connected to the input end of the pnp Darlington circuit, a source of the PMOS transistor connected to a control end of the pnp Darlington circuit, a gate of the PMOS transistor connected to the output end of the pnp Darlington circuit. It is implicitly disclosed because given a circuit between the voltages +V and 0 volts, it is well known in the art that structure of the circuit symmetrically connected between 0 and –V volts will function identically. Having taken into consideration inverting the polarities of the components npn to pnp, for example, these components are art recognized equivalents used for the same intended purpose.

Claims 2, 3 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ker et al. (US 6072219) in view of Voldman et al. (US 6549061) and Glica (US 5262689) and Williams et al. (US 5485027).

Regarding claim 2 Ker et al. in view of Voldman et al. discloses the electrostatic discharge protection circuit of claim 1.

Ker et al. in view of Voldman et al. does not disclose wherein the npn Darlington circuit further comprises two npn-type bipolar junction transistors (BJTs), each npn BJT comprising an N+ buried layer, a P well formed on the N+ buried layer, an N well formed on the N+ buried layer around the P well, and an N+ node formed in a top side of the P well; and the NMOS transistor comprises an N+ buried layer, a P well formed on the N+ buried layer, an N well formed on the N+ buried layer around the P well, and two N+ nodes formed in a top side of the P well.

Firstly, Glica teaches wherein the npn Darlington circuit further comprises two npn-type bipolar junction transistors (BJTs) (a darlington consists of two transistor equally constructed connected in tandem configuration), each npn BJT comprising an N+ buried layer (Fig. 3B), a P well formed on the N+ buried layer (fig. 3B), an N well formed on the N+ buried layer around the P well (Fig. 3B element NBODY), and an N+ node formed in a top side of the P well (Fig. 3B element N+).

Secondly, Williams et al. teaches wherein the NMOS transistor comprises an N+ buried layer (Fig. 22 element 123), a P well formed on the N+ buried layer (Fig. 22 element 201), an N well formed on the N+ buried layer around the P well (Fig. 22 element 203), and two N+ nodes (Fig. 22 elements 211, 213) formed in a top side of the P well.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ker et al. in view of Voldman et al. device with the teachings of Glica because the theory of fabrication of semiconductors using the P and N elements by combining them with different impurity concentrations is known to be a method of producing smaller solid state devices that are compatible with the smaller elements currently being used in computer systems and devices.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ker et al. in view of Voldman et al. device with the teachings of Williams et al. because the theory of fabrication of semiconductors using the P and N elements by combining them with different impurity concentrations is known to be a method of producing smaller solid state devices that are compatible with the smaller elements currently being used in computer systems and devices.

Regarding claim 3 Ker et al. in view of Voldman et al. and Glica and Williams et al. discloses the electrostatic discharge protection circuit of claim 2.

Williams et al further teaches how to accomplish the so-called "***Self Isolation***" which is applied in the two BJTS and the NMOS transistor are formed on a P-substrate, and the N wells of the two npn BJTS and the NMOS transistor are used to isolate the P wells and the P-substrate (Col. 1 lines 28-30).

Claims 7 & 8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Ker et al. (US 6072219) in view of Voldman et al. (US 6549061) and Li (US 6496055) and Chen et al. (US 5790460).

Regarding claim 7 Ker et al. in view of Voldman et al. discloses the electrostatic discharge protection circuit of claim 1.

Ker et al. in view of Voldman et al. does not disclose wherein the npn Darlington circuit further comprises two npn BJTS, each npn BJT comprising a deep N well, a P well formed on the deep N well, and an N+ node formed in a top side of the P well; and the NMOS transistor comprises a deep N well, a P well formed on the N well, and two N+ nodes formed in a top side of the P well.

Firstly, Li teaches wherein the npn Darlington (a darlington consists of two transistor equally constructed connected in tandem configuration) further comprises two npn BJTS, each npn BJT comprising a deep N well (Fig. 5 element 526), a P well formed on the deep N well (fig. 5 element 522), and an N+ node formed in a top side of the P well (Fig. 5 element 518).

Secondly, Chen et al. teaches wherein the NMOS transistor comprises a deep N well (Col. 3 lines 66-67 & col. 4 line 1 & Fig. 3 element 25a), a P well formed on the N well (Col. 3 lines 66-67 & col. 4 line 1 & Fig. 3 element 22a), and two N+ nodes formed in a top side of the P well (Col. 3 lines 66-67 & Col. 4 line 1 & Fig. 3 elements 30a, 31a)
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ker et al. in view Voldman device with the teachings of Li because the theory of fabrication of semiconductors using the P and N elements by combining them with different impurity concentration is known to be a method of producing smaller solid state devices that are compatible with the smaller elements currently being used in computer systems and devices.
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ker et al. in view of Voldman et al. device with the teachings of Chen et al. because the theory of fabrication of semiconductors using the P and N elements by combining them with different impurity concentration is known to be a method of producing smaller solid state devices that are compatible with the smaller elements currently being used in computer systems and devices.

Regarding claim 8 Ker et al. in view of Voldman et al. and Li and Chen et al. discloses the electrostatic discharge protection circuit of claim 7
Chen et al. further discloses (for the NMOS, which can also be applied to the Darlington) wherein the two BJTS and the NMOS transistor are formed on a P-substrate, and the deep N wells of the two npn BJTS and the NMOS transistor are used to isolate the P wells and the P-substrate (Col. 3 lines 66-67 & Col. 4 line1).

Regarding claims 6 & 9, none of the references discloses a BiCMOS or CMOS process. However in apparatus claims, the method of forming the apparatus is not germane to the issue of patentability of the apparatus itself as patentability is determined based on the recited structural components of the apparatus.

Claim 13 is rejected under 35 U.S.C. §103(a) as being unpatentable over Ker et al. (US 6072219) in view of Voldman et al. (US 6549061) and Chen et al. (US 5671111).

Regarding claim 13 Ker et al. discloses an electrostatic discharge protection circuit (Abstract) comprising: an P-type channel metal-oxide semiconductor (PMOS) transistor (Fig. 10 element P1), a drain of the PMOS transistor connected to the output end of a clam circuit (Fig. 10) a source of the PMOS transistor connected to a control end of the pnp Darlington circuit (Fig. 10 connection between P1, R2 going to B2), a gate of the PMOS transistor connected to the input end of a clamp circuit.

Ker et al. does not disclose wherein the clamp circuit is a Darlington circuit comprising a input end and an output end.

Voldman et al. teaches wherein a clam circuit is an npn Darlington circuit (Fig. 6 element 604) comprising a input end (Fig. 6 element 210) and an output end (Fig. 6 element 212), the output end of the npn Darlington circuit being grounded (Fig. 6 element 212). This Darlington connected at the bottom half of the circuit 10 disclosed by Ker et al.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Ker et al. device with the Voldman et al. Darlington features. Both teachings are in the ESD area, which have a main purpose to reduce the impedance between the input pad and the power source (i.e. discharge of current between the input to the power source). Furthermore, a Darlington offers the advantage of driving/supporting higher magnitudes of current than a single transistor, because it has a gain equals to $\beta^2 = \beta_1 . \beta_2$ (where $\beta 1$ and $\beta 2$ correspond to the gains of each transistor).

Ker et al. does not disclose wherein the clamp circuit is a pnp Darlington circuit comprising a input end and an output end.

Chen et al. teaches an ESD circuit with an NMOS and PMOS transistor each connected to a correspondent clamp circuit (Fig. elements 130, 135). The bipolars transistors of each half have opposite polarity pnp or npn depending on which half are they connected.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the Ker et al. device with the Chen et al. Darlington features. Both teachings are in the ESD area, which have a main purpose to protect the apparatus from discharge of current between the input to the power source. It is obvious to connect the bipolar transistors with the right polarity in each half, so they provide the functionality required.

Allowable Subject Matter

Claims 4 & 5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to teach or fairly suggest the specific configuration or way of manufacturing the devices described in these dependent claims.

Applicant's arguments with respect to claims 1-3, 7, 8 & 10-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luis E. Román whose telephone number is (571) 272 – 5527. The examiner can normally be reached on Mon – Fri from 7:15 AM to 3:45 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571) 272-2800 x 36. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from Patent Application Information Retrieval (PAIR) system.

Status information for unpublished applications is available through private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LR/050306

Luis E. Román

Patent Examiner

Art Unit 2836

BRIAN SIRCUS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800